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Figure 1 Typical overlay patterns or completed alignment attributes

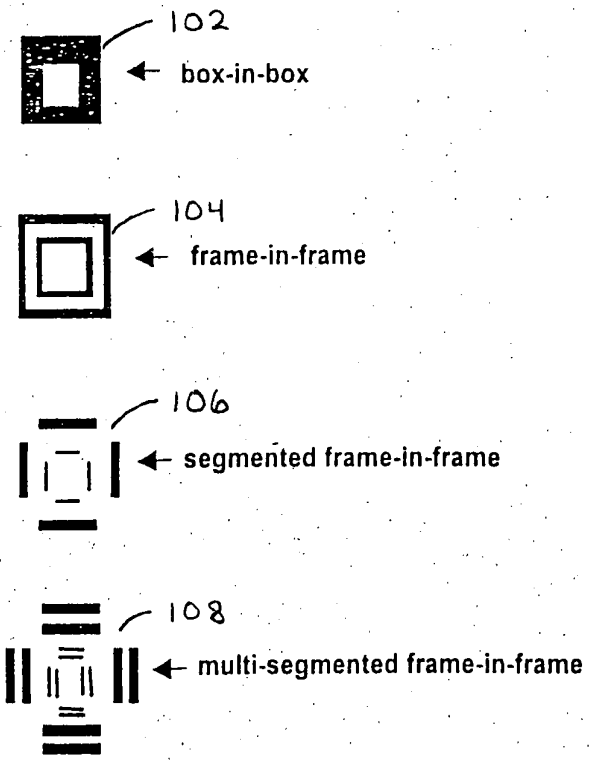

Figure 2 Typical optical verniers

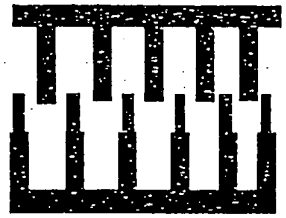

Figure 3 Reticle

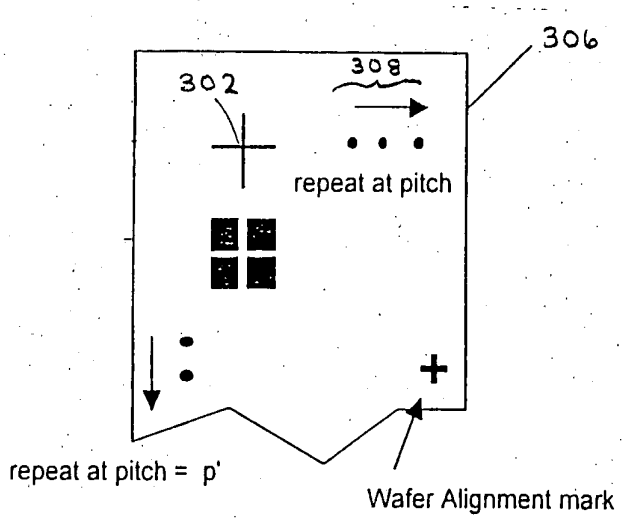

Figure 4 Overlapped male and female target pairs

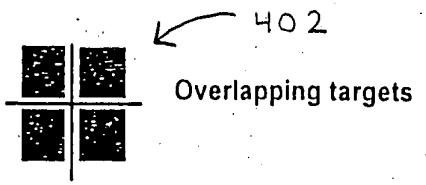

Figure 5A Detail of reticle fo figure 3

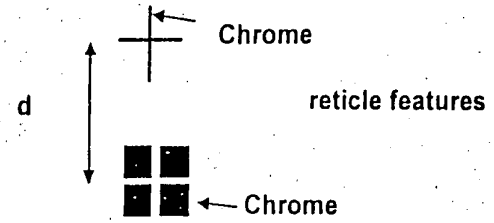

Figure 5B Features of figure 5
in developed positive photoresist

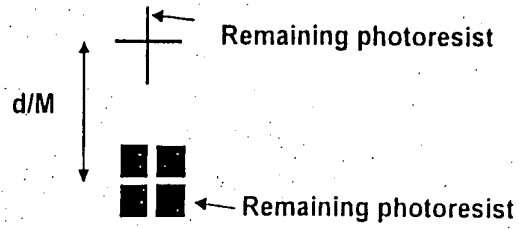

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Figure 6 An embodiment process flow for creating reference wafer

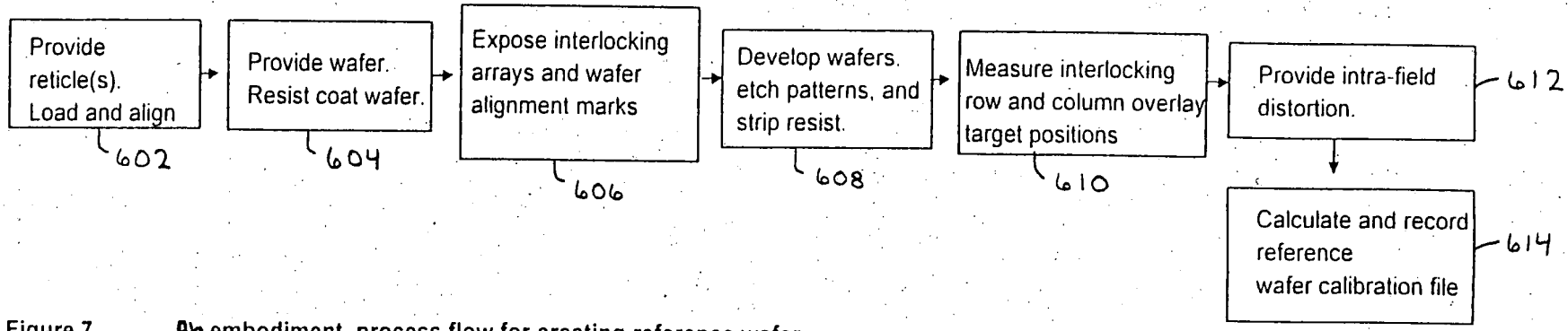

Figure 7 An embodiment process flow for creating reference wafer

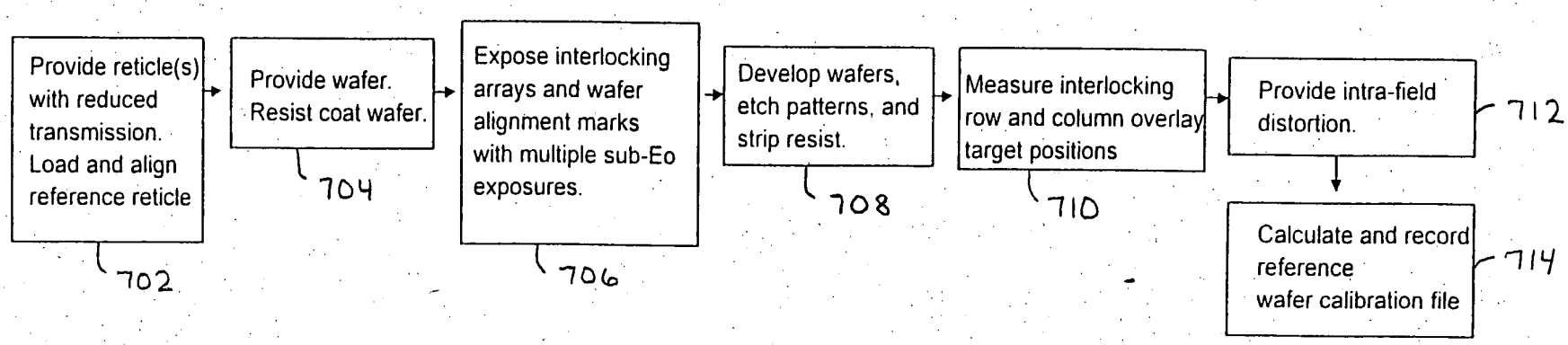

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Figure 8 Example application of reference wafer

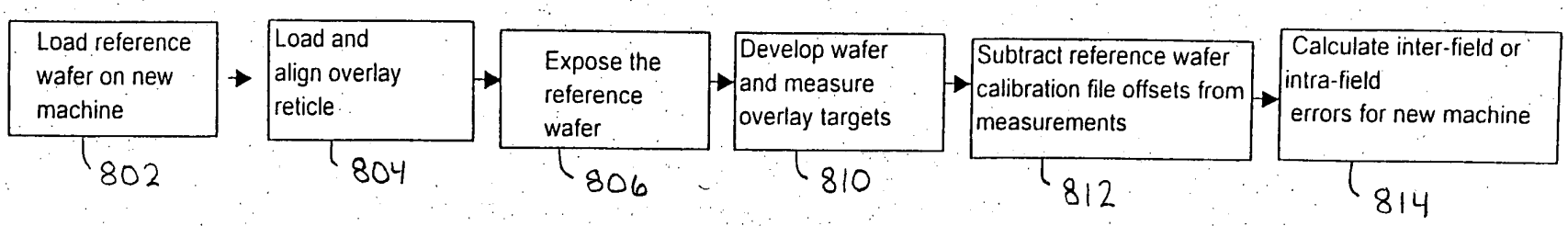
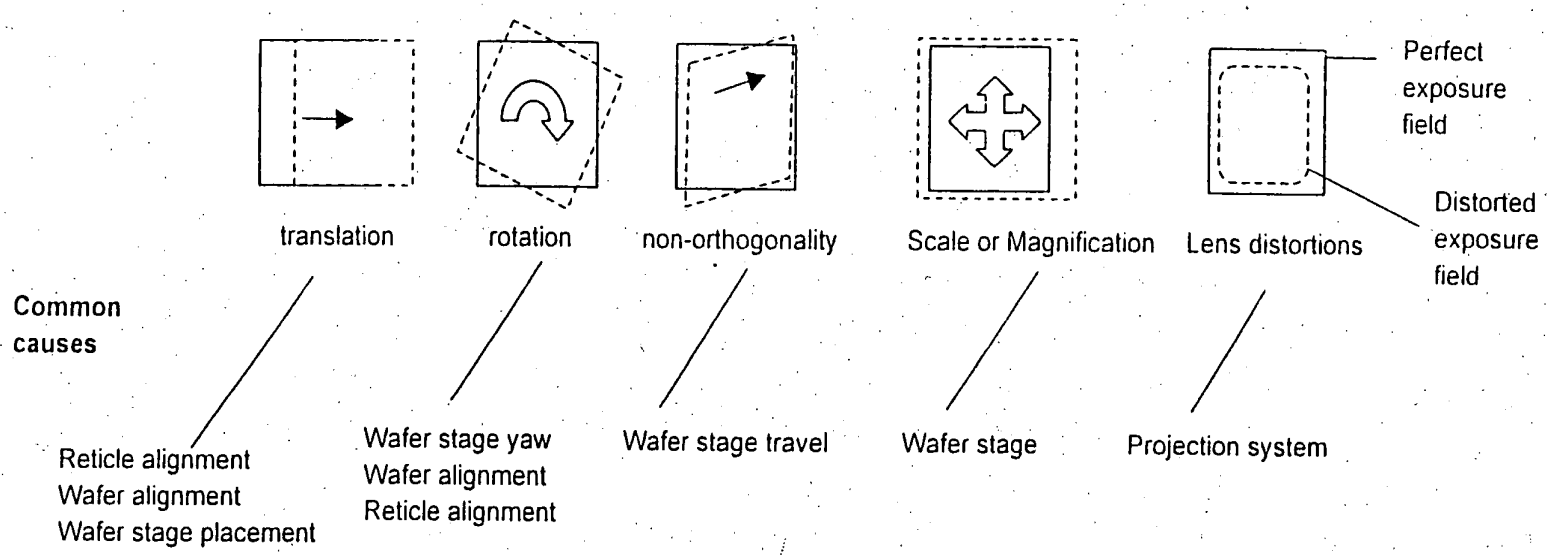


Figure 9 Common causes of overlay or placement error (Inter-field and Intra-field)



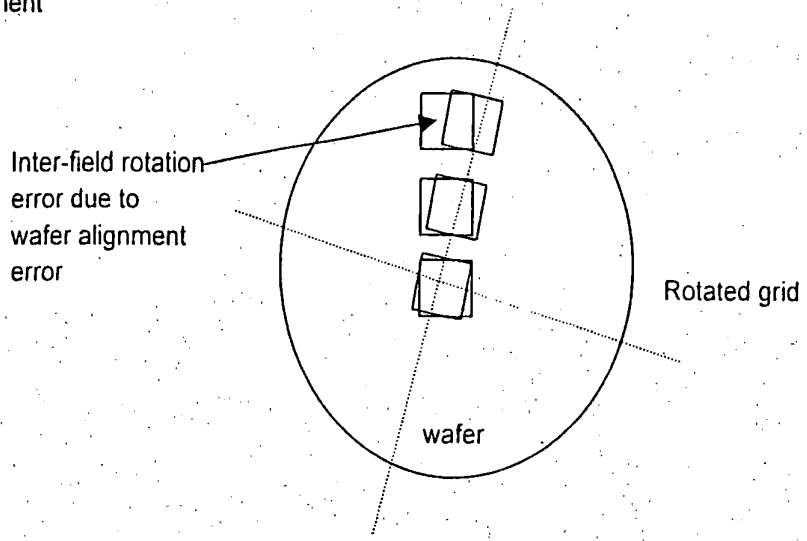


Figure 10 Photolithographic stepper or scanner system

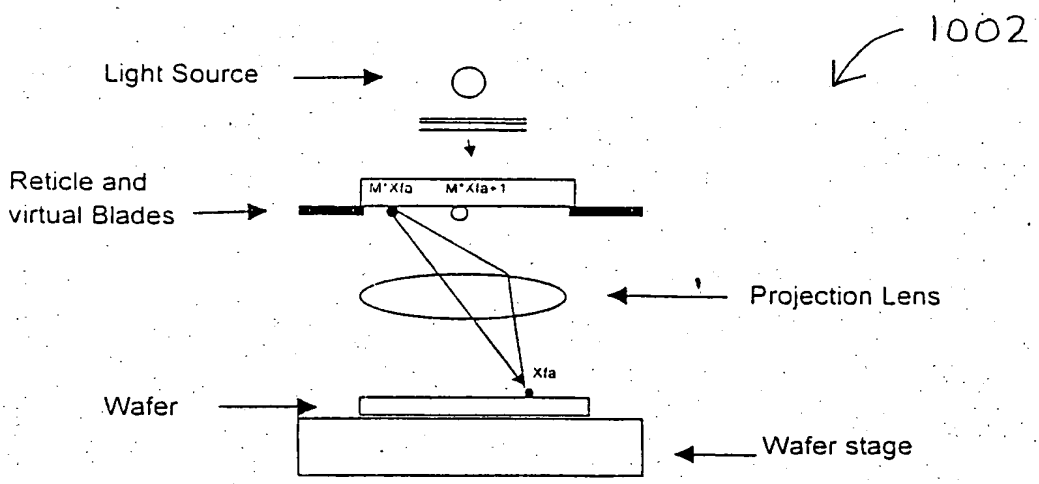


Figure 11A Inter-field and intra-field overlay error

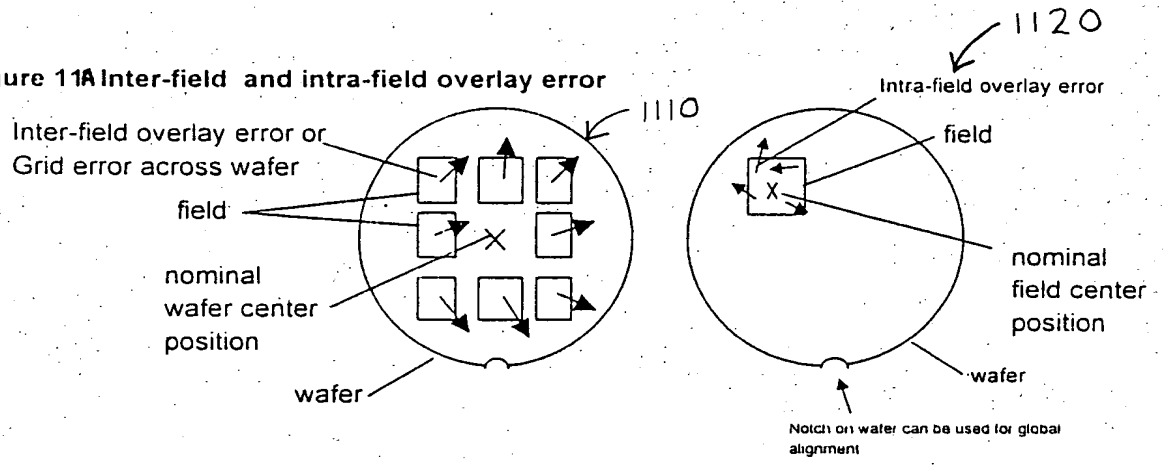


Figure 11B Interfield Yaw error

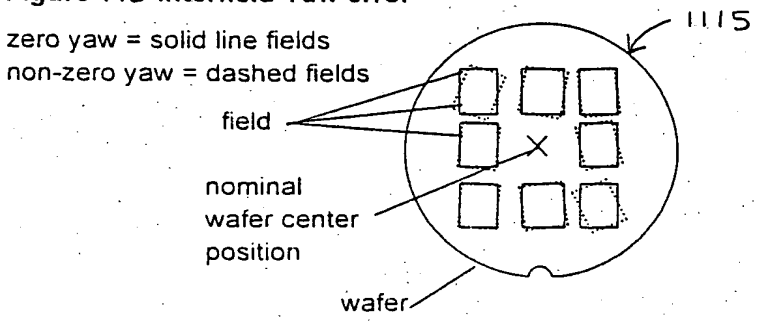


Figure 12 Detail of interlocking fields in X and Y directions on the reference wafer, 3 fields shown.
Solid lines = field (i, j)
Dashed lines = field (i, j+1)
Dotted lines = field(i+1, j)
Filled squares = field (i+1, j+1)
Sx = X field pitch = Nx*P/M
Sy = Y field pitch = Ny*P/M

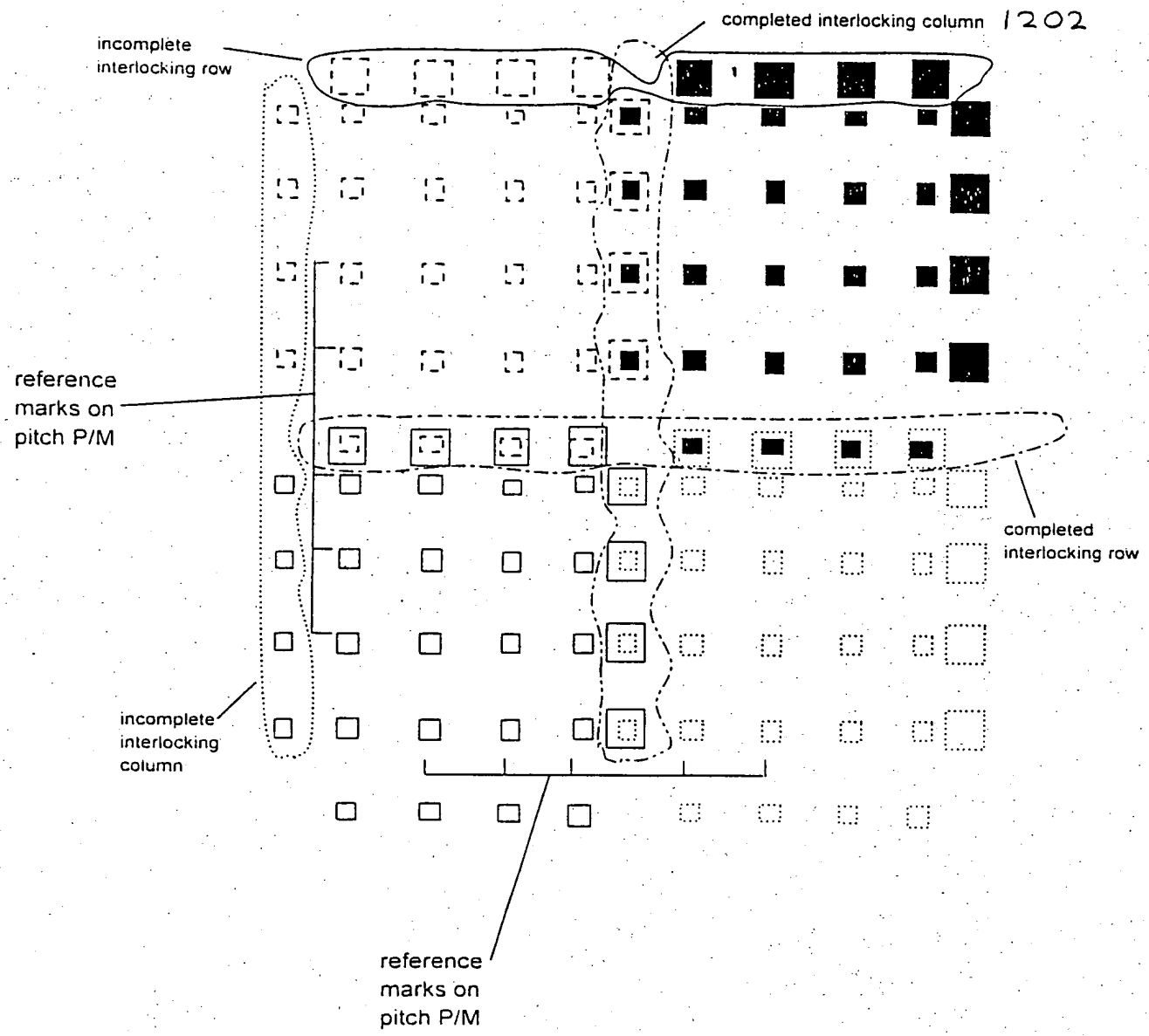


Figure 13A Reference reticle of the present invention. This reticle contains a complete Nx x Ny interlocking array and no wafer alignment marks.

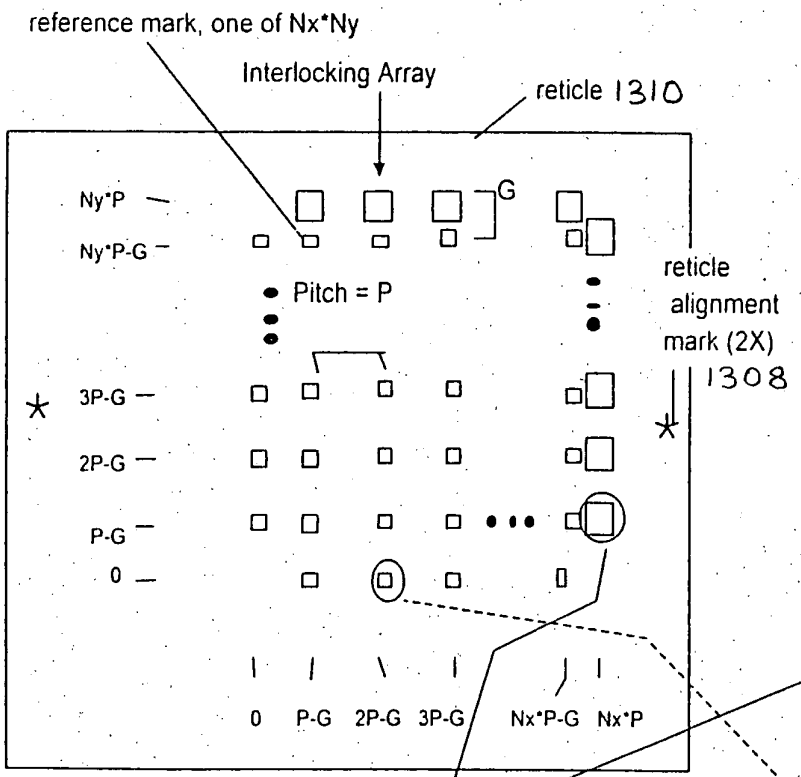
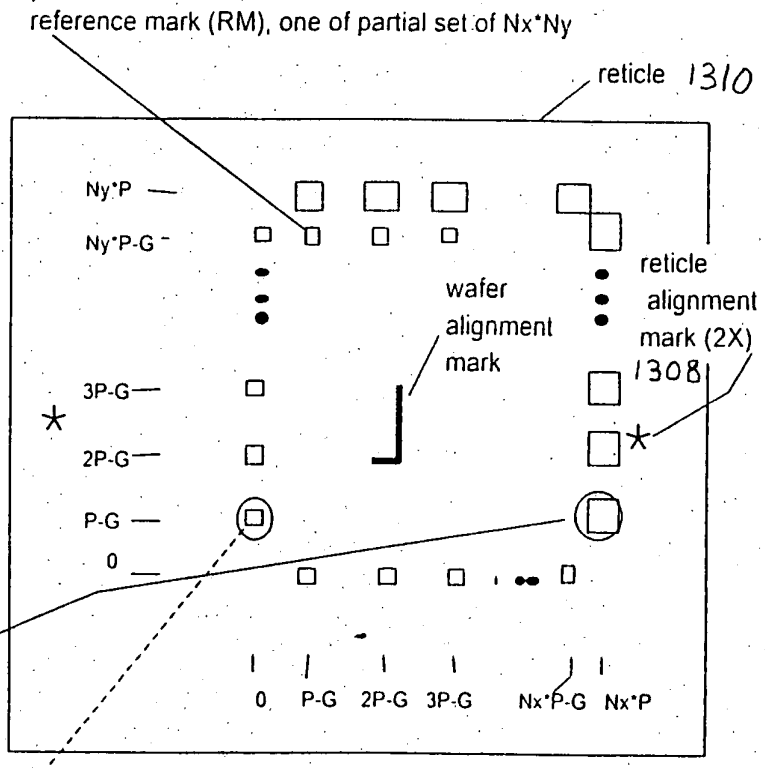


Figure 13B Reference reticle containing wafer alignment marks , portion of interlocking array and complete interlocking rows and columns. One reticle of a set.



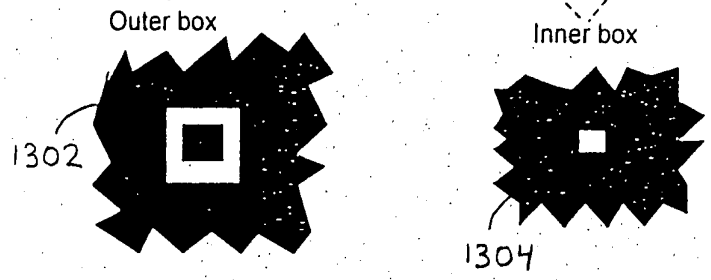
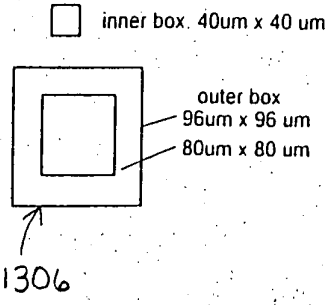


Figure 13C Exemplary inner and outer box sizes. Design of figure 13A and 13B, um = microns.



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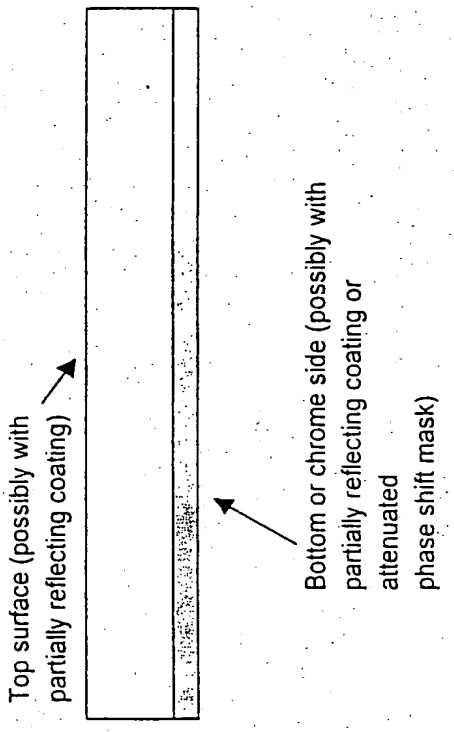


Figure 14 Side view of reference reticle

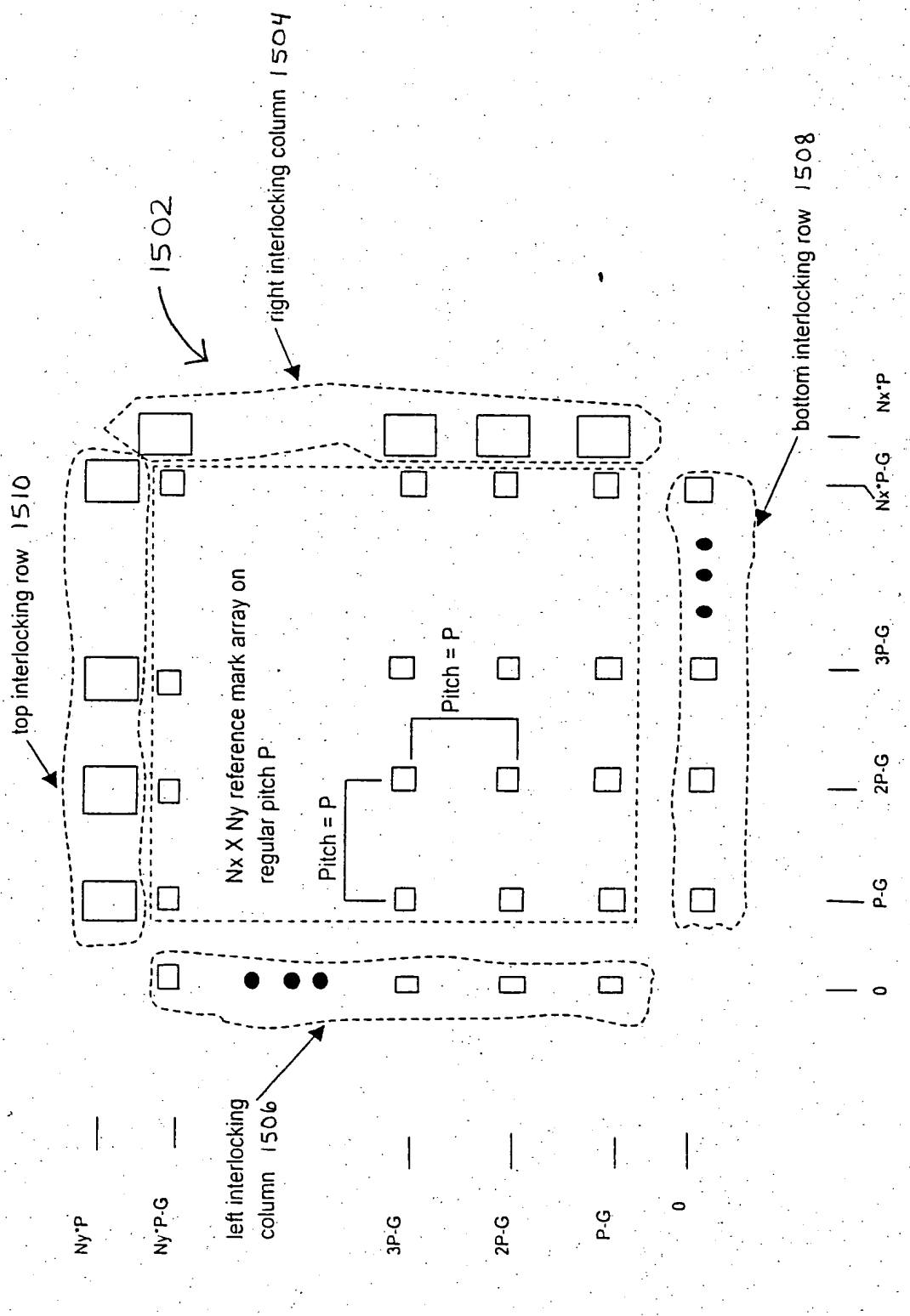


Figure 15 Further explanation of the components of the interlocking array of the reference reticle of figure 13A

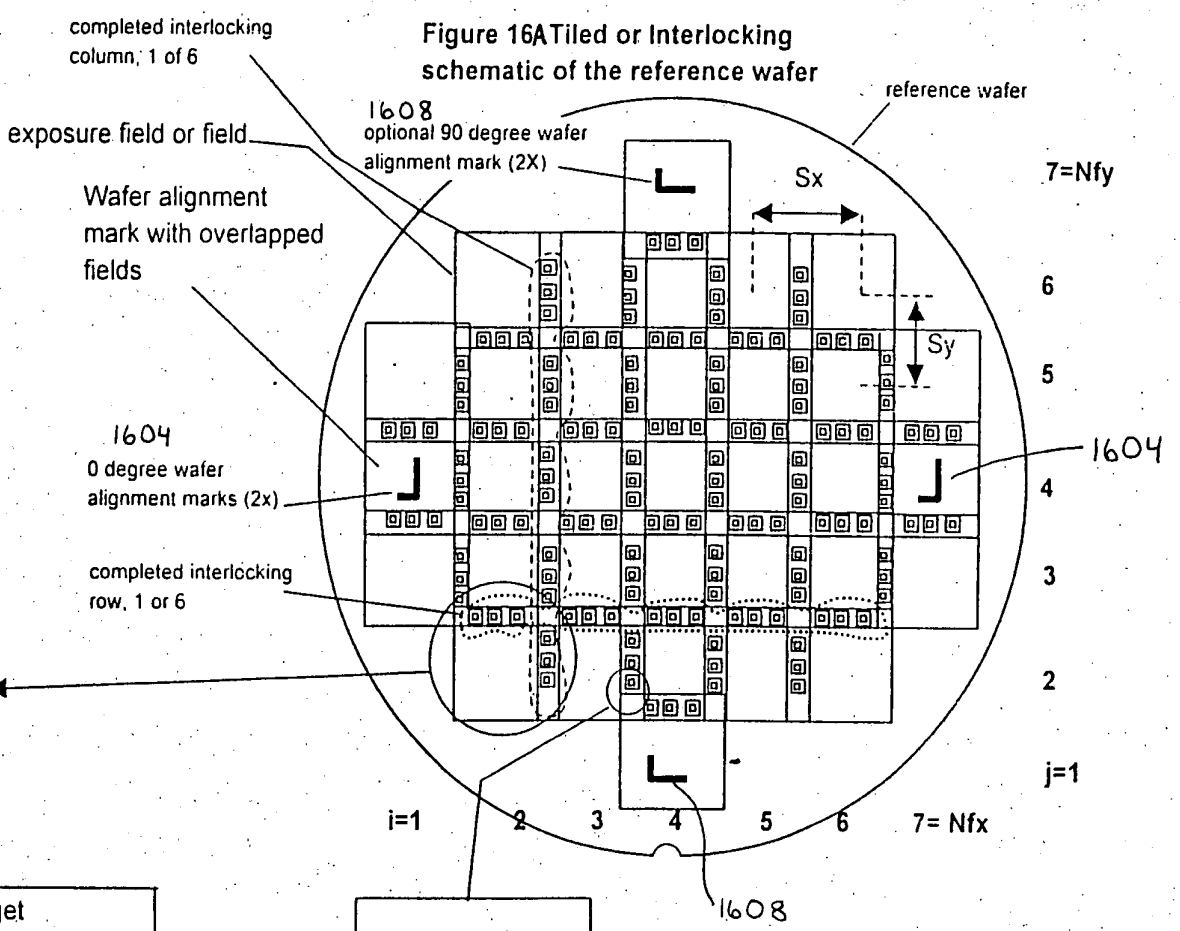


Figure 16A Tiled or Interlocking schematic of the reference wafer

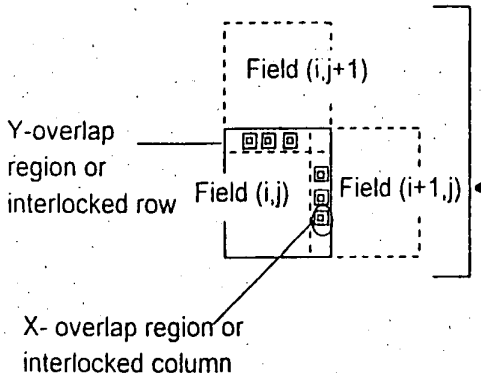


Figure 17A Typical overlapping regions showing 3 box-in-box overlay targets

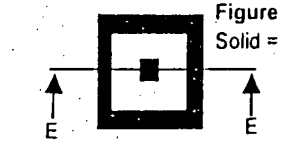


Figure 16B Plan view of interlocking measurement site. Solid = etched region, White = unetched

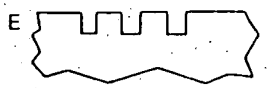


Figure 16C Cross sectional view of interlocking measurement site of figure 16A

Figure 17B Perfectly centered overlay target box measurement site and sign for displacement.

Figure 18 Overlay error vector plot

Figure 19 Translation overlay vector plot

Figure 20 Rotation overlay vector plot

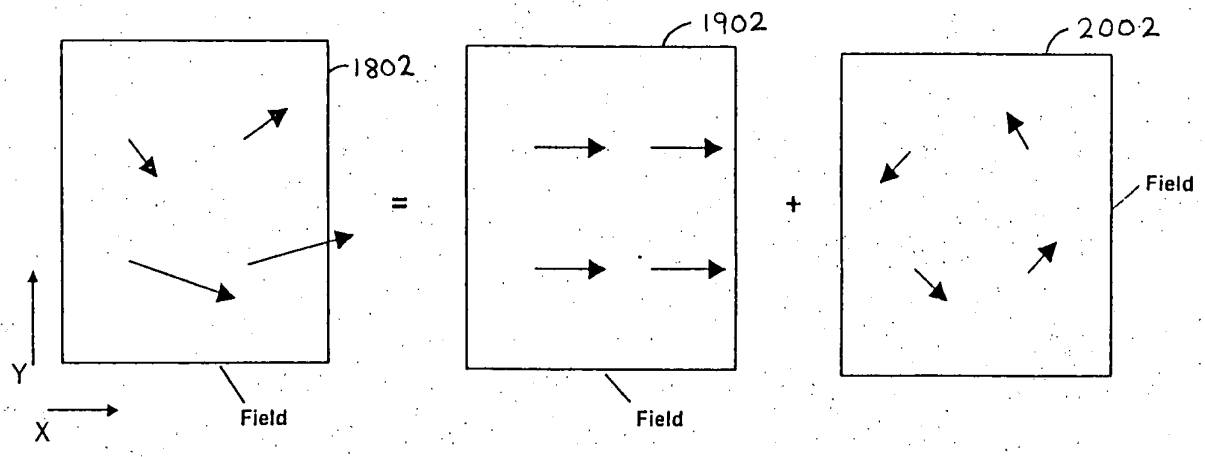
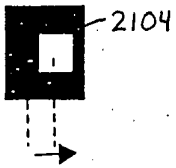
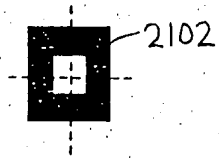


Figure 21 Overlay measurement notation



The vector represents the alignment offset distance between the box-in-box structure



Perfectly centered box in box structure

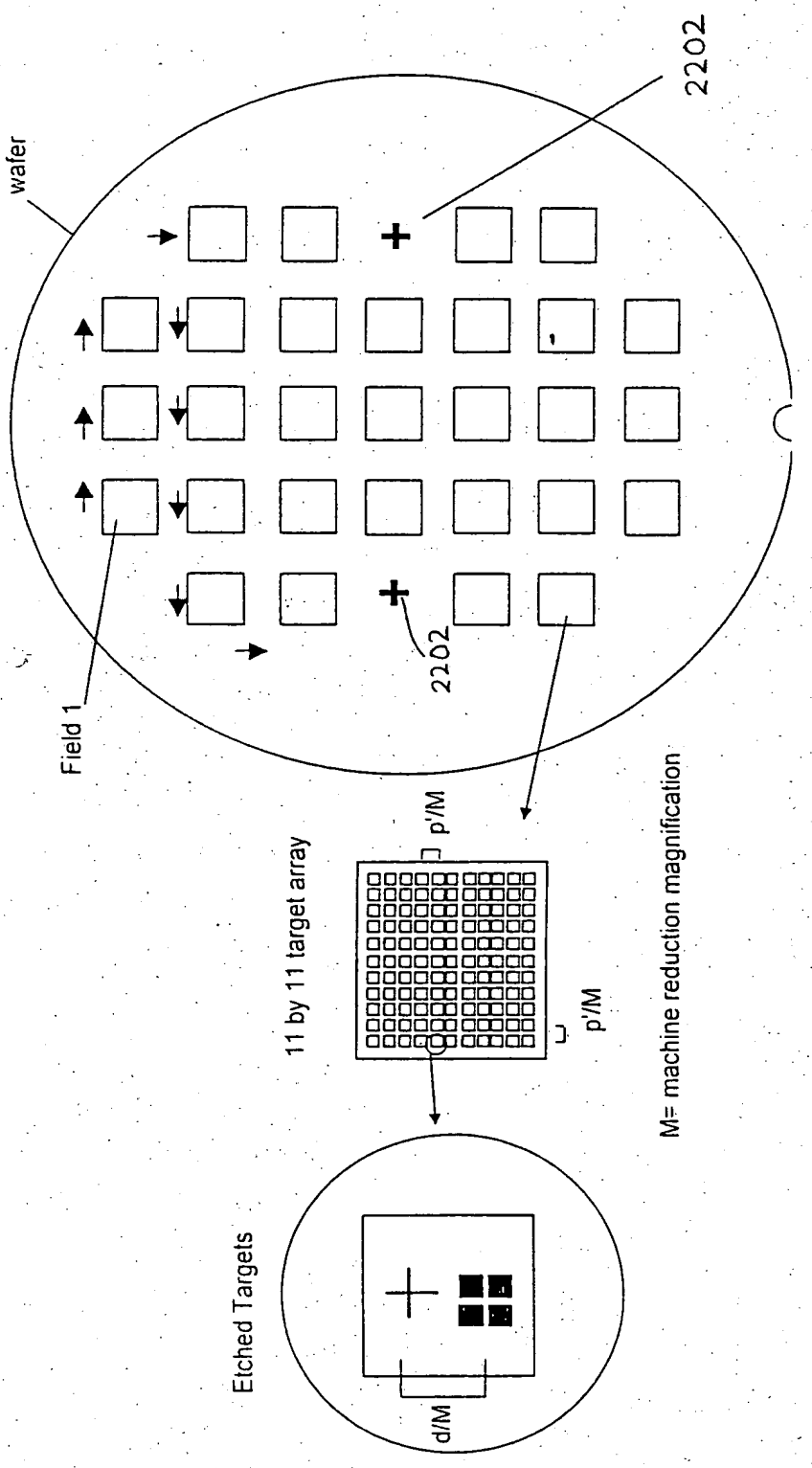


Figure 22 Golden wafer

Figure 23 Wafer alignment mark reticle

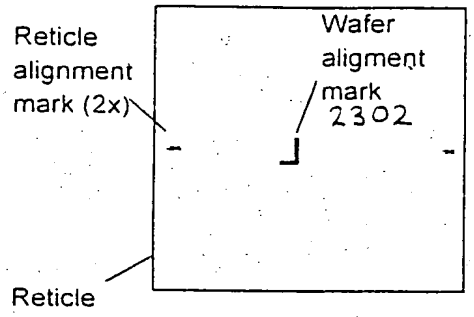


Figure 24 Inner box reticle

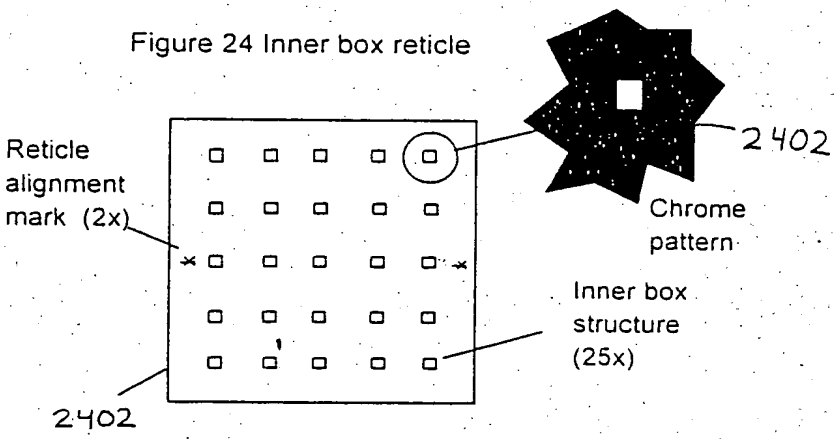
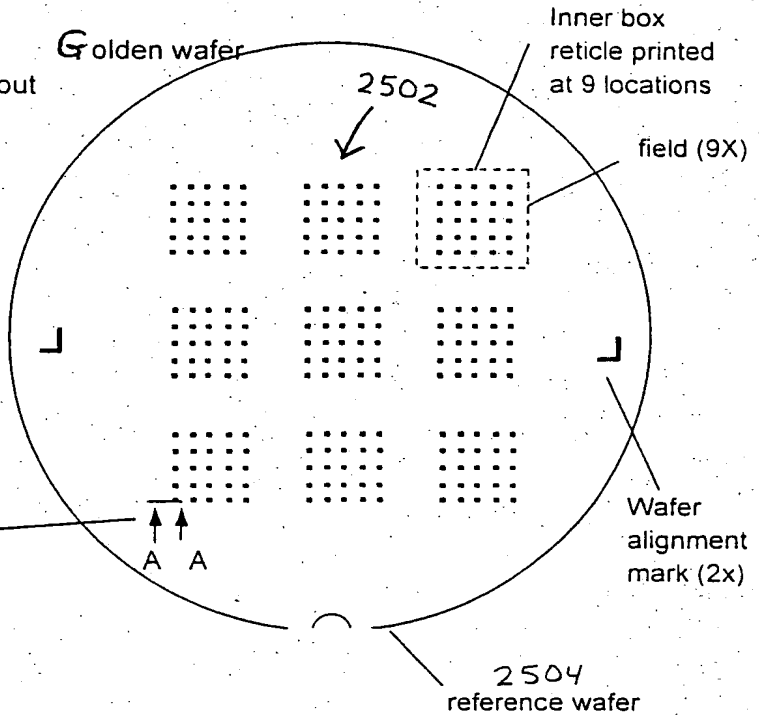


Figure 25 Golden wafer layout



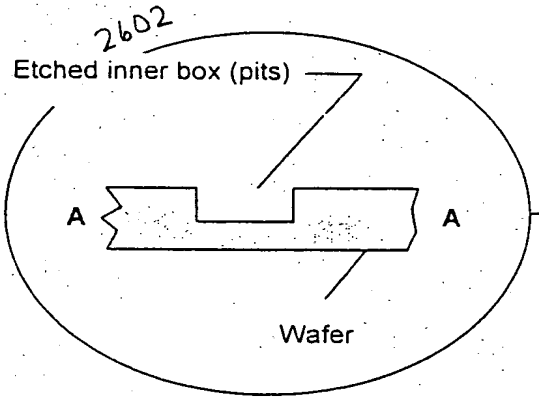


Figure 26 Cross section of inner box

Figure 27 Outer box reticle schematic

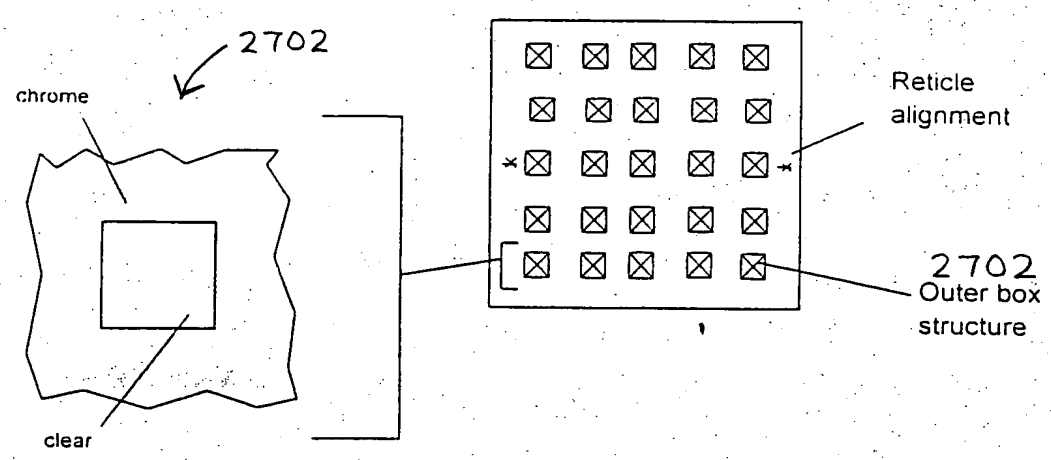


Figure 28 Outer box reticle detail

Figure 29 Golden wafer ready for overlay measurement

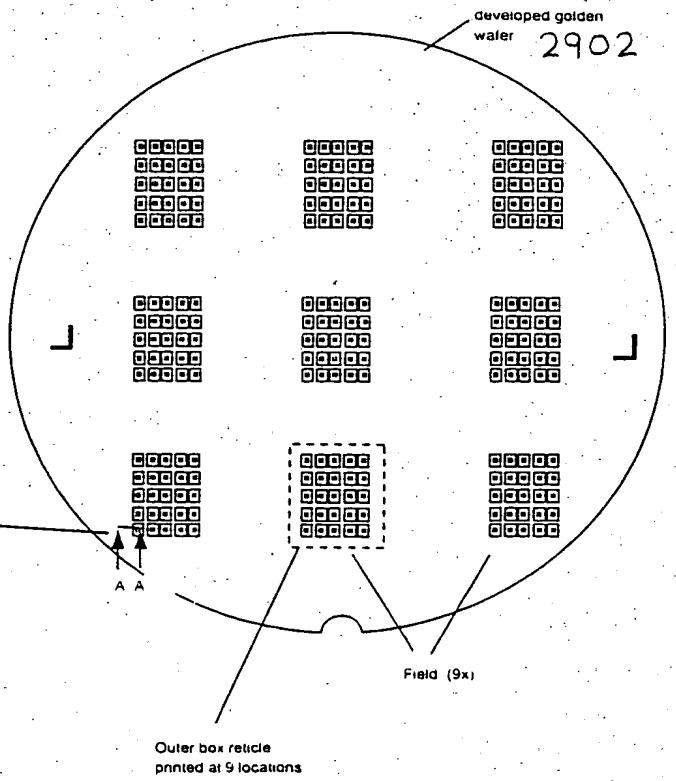
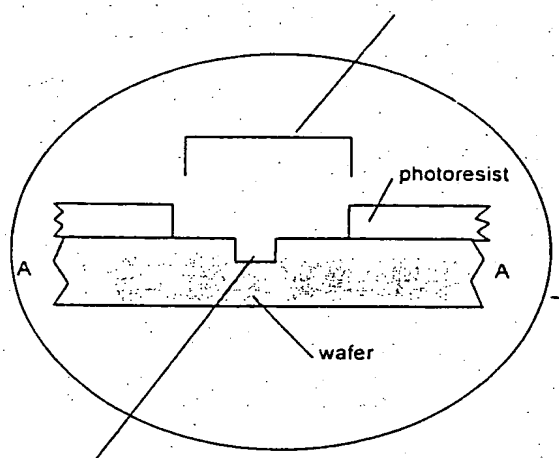


Figure 30 Box-in-Box cross-section AA



Etched inner box from reference stepper or scanner

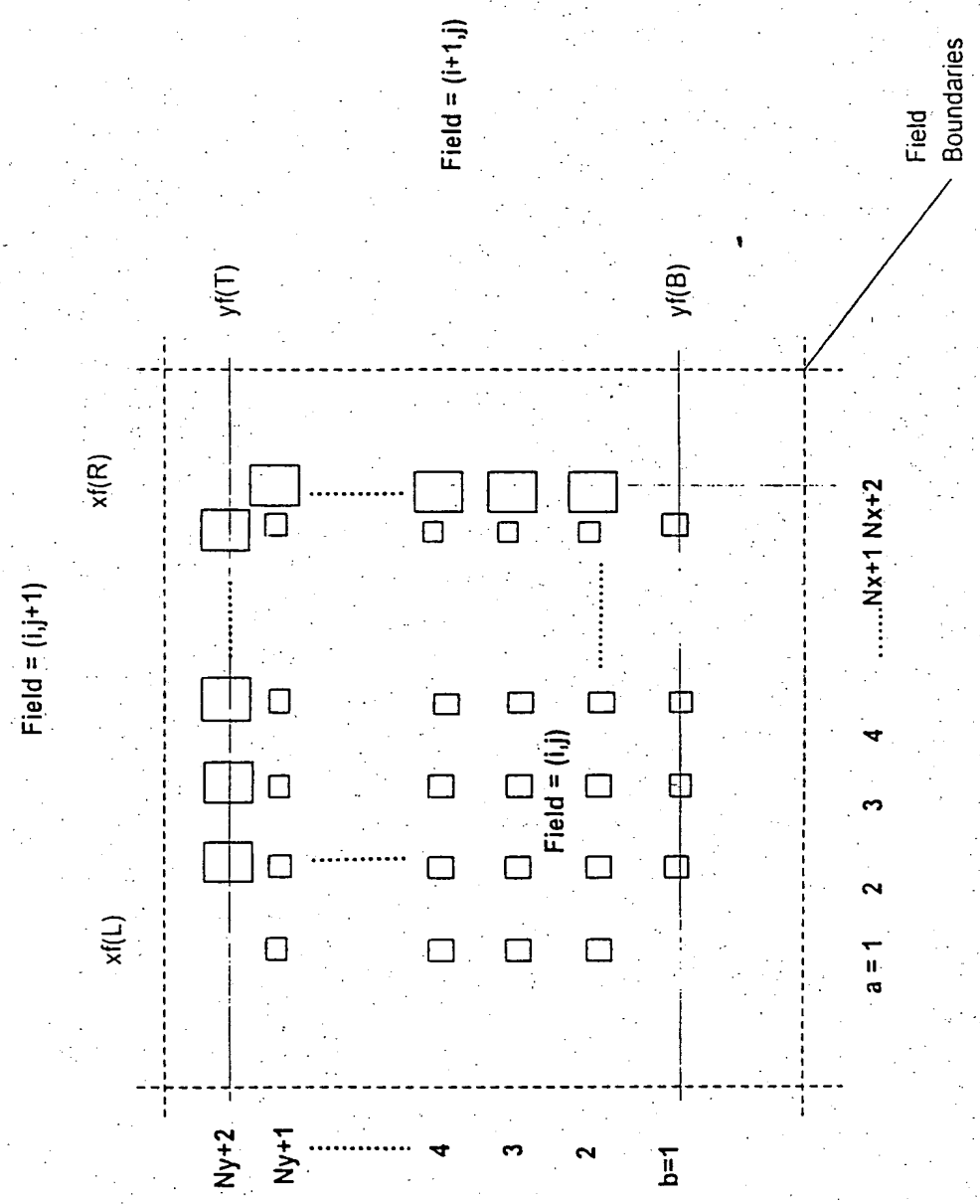


Figure 31 Inter-field and Intra-field indices

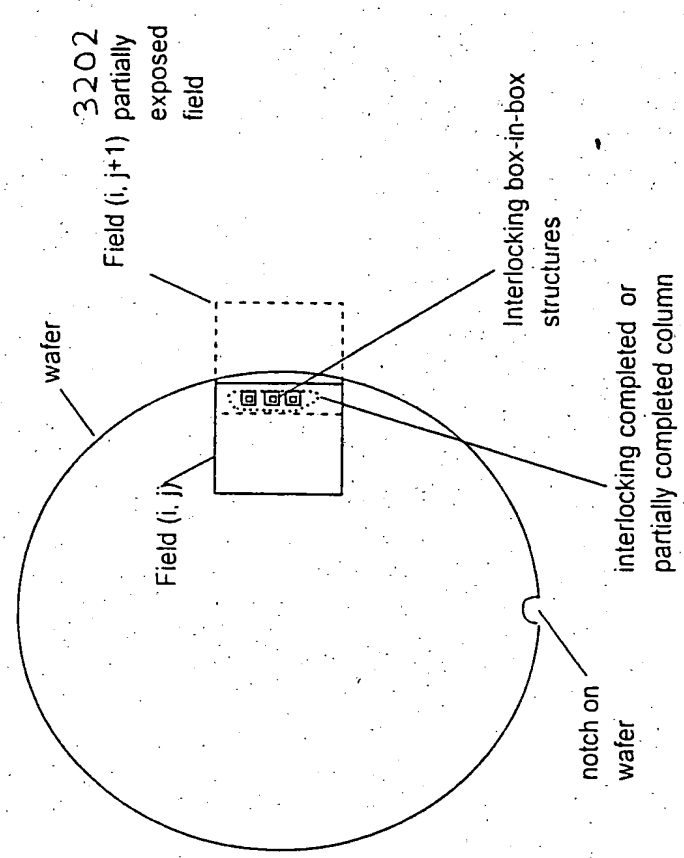


Figure 32 Partially exposed field and interlocking box-in-box structures along Field (i,j+1)s' left edge

Figure 33 Operational portions of completed reference wafer

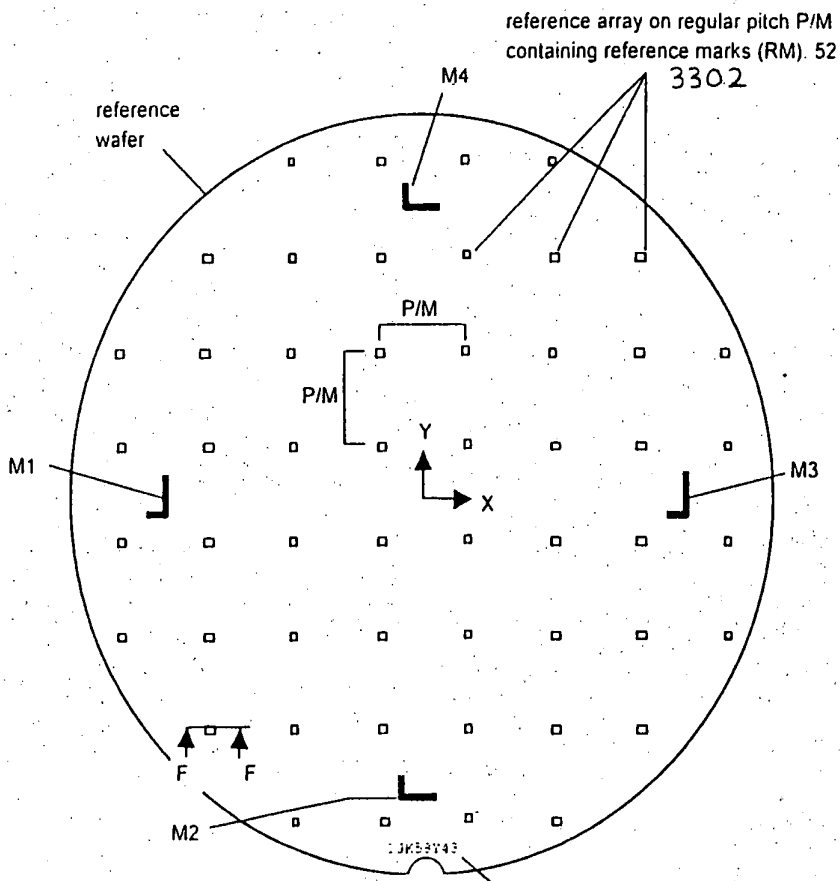


Figure 34 Exemplary calibration file for reference wafer of figure 33 (units = mm).

Feature	xG	yG	dx	dy
M1	-95.000000	0.000000	0.000050	-0.000037
M2	0.000000	-95.000000	-0.000387	0.000298
M3	95.000000	0.000000	0.000499	-0.000399
M4	0.000000	95.000000	0.000174	0.000274
RM	10.000000	10.000000	0.000598	0.000420
RM	10.000000	20.000000	0.000495	-0.000229
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
RM	-60.000000	-80.000000	0.000339	0.000449

52 entries
for wafer of
figure 33

Figures 35A:35F show cross section FF of Figure 33 and details a variety of vertical structures possible for the reference mark (RM).

= Si or substrate

= deposited of overcoat layer

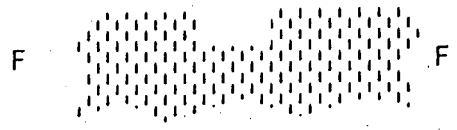


Figure 35A Pits in wafer

Figure 35B Pits in overcoating

Figure 35C Pits in overcoating and wafer

Figure 35D Pits in wafer overcoated

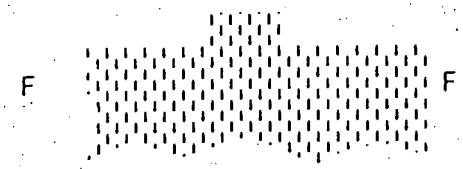


Figure 35E Mound in wafer

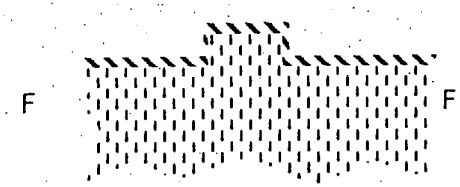


Figure 35F Overcoated mound on wafer

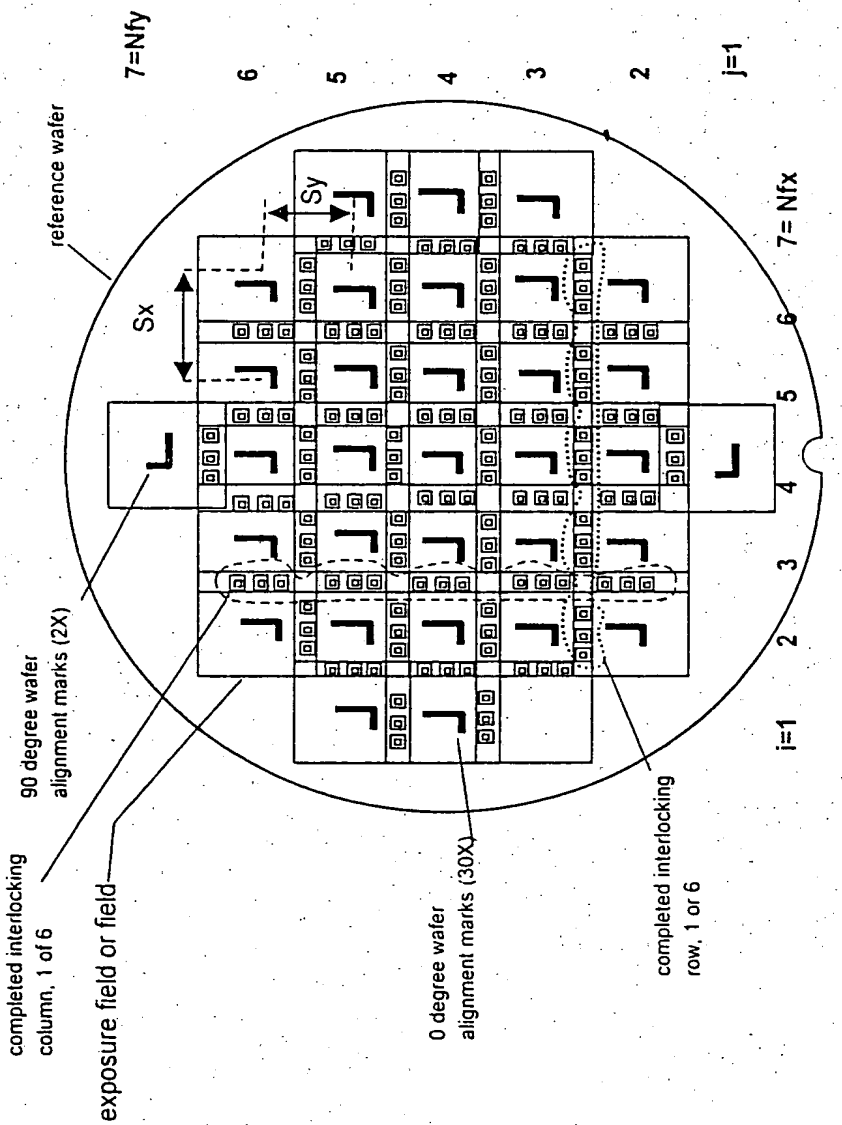


Figure 36 Tiled or interlocking schematic for reference wafer containing only wafer alignment marks and interlocking rows and columns.